CLAIMS

What is claimed is:

1. A method of compiling a circuit interconnect model, comprising:
providing extraction data from an interconnect;
reading a dataset from said extraction data from said interconnect;
reducing said dataset to form a model;
evaluating said model for a set of conditions to obtain a solution; and
writing said solution to an application.

2. The method of claim 1, further comprising, after reducing said dataset to form a model, writing said model to a parasitic database and, before evaluating said model, reading said model from said parasitic database.

3. The method of claim 2, wherein writing said dataset to said parasitic database includes using a view translator plug-in.

4. The method of claim 1, further comprising providing a circuit database and writing a name map.

5. An electronic media, comprising a program for performing the method of claim 1.

6. A computer program, comprising computer or machine readable program elements translatable for implementing the method of claim 1.

7. An integrated circuit designed in accordance with the method of claim 1.

8. The method of claim 1, further comprising verifying a design of an integrated circuit.

9. A computer program comprising computer program means adapted to perform the steps of providing extraction data from an interconnect; reading a dataset from said extraction data from said interconnect; reducing said dataset to form a model; evaluating said model for a set of conditions to obtain a solution; and writing said solution when said program is run on a computer.

10. A computer program as claimed in claim 9, embodied on a computer-readable medium.